



S/N 09/259,849

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Paul A. Farrar

Examiner: Ginette Peralta

Serial No.: 09/259,849

Group Art Unit: 2814

Filed: March 1, 1999

Docket: 303.557US1

Title: CONDUCTIVE STRUCTURES IN INTEGRATED CIRCUITS

COMMUNICATION CONCERNING RELATED APPLICATION(S)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicant would like to bring to the Examiner's attention the following related application(s) in the above-identified patent application:

<u>Serial/Patent No.</u>	<u>Filing Date</u>	<u>Attorney Docket</u>	<u>Title</u>
09/032197 6211073	February 27, 1998	303.459US1	METHODS FOR MAKING COPPER AND OTHER METAL INTERCONNECTIONS IN INTEGRATED CIRCUITS
09/817447	March 26, 2001	303.459US2	METHODS FOR MAKING COPPER AND OTHER METAL INTERCONNECTIONS IN INTEGRATED CIRCUITS
09/128859 6284656	August 4, 1998	303.473US1	COPPER METALLURGY IN INTEGRATED CIRCUITS
09/946055 6614099	September 4, 2001	303.473US2	COPPER METALLURGY IN INTEGRATED CIRCUITS
09/145012 6288442	September 1, 1998	303.505US1	INTEGRATED-CIRCUIT WITH OXIDATION-RESISTANT POLYMERIC LAYER
09/256123 6211049	February 24, 1999	303.505US2	FORMING SUBMICRON INTEGRATED-CIRCUIT WIRING FROM GOLD, SILVER, COPPER AND OTHER METALS

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Page 2

Dkt: 303.557US1

09/256124 6208016	February 24, 1999	303.505US3	FORMING SUBMICRON INTEGRATED-CIRCUIT WIRING FROM GOLD, SILVER, COPPER AND OTHER METALS
09/789091	February 20, 2001	303.505US4	INTEGRATED-CIRCUIT WITH OXIDATION-RESISTANT POLYMERIC LAYER
10/117041	April 5, 2002	303.673US2	INTEGRATED CIRCUIT AND SEED LAYERS

Respectfully submitted,

PAUL A. FARRAR

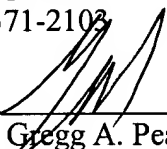
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By


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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 12 day of July, 2004.

Name



Signature

